IN THE SPECIFICATION

Please amend the title to read:

Using a Plurality of Processing Elements ~~Data Driven Digital Signal Processor~~.

Please amend the paragraph beginning on page 5, line 26, as follows:

The register 16 includes a bus interface 34 and N general purpose registers 32 configured to allow independent read and write operations that can occur from a number of processing elements 12 at the same time. The GPR 32 allows independent data transfers from ~~and to~~ any of the other processing elements 12 and to any of the other processing elements 12. The GPR 32 includes registers for each of the processing elements 12 that can be written to by any processing element 12. If two processing elements 12 try to write to the same register, an error flag is set.